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PATENT APPLICATION

DUAL STACKED DIE PACKAGE

Inventor:

Maria Cristina B. Estacio, a citizen of Philippines, residing at,
Phase 2B, Blk 5, Lot 22
Villa Leyson
Cebu City
Philippines

Assignee:

Fairchild Semiconductor Corporation
82 Running Hill Road
South Portland, ME 04106

Entity: Large

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: 415 578-0200

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BACKGROUND OF THE INVENTION

1. Background of the Invention

The present invention relates to a semiconductor device, and more particularly, to packaging techniques for semiconductor devices that include a package that can accommodate dual stacked dies.

2. Description Of The Prior Art

Many of the applications for today's semiconductor devices require more and more power or capacity. However, today's applications also prefer semiconductor packages that are compact and thin. Finally, a concern in improving semiconductor devices includes maintaining very low package resistance (RDSon).

SUMMARY OF THE INVENTION

The present invention provides a semiconductor device that includes a leadframe that has a first source attach area on a first surface of the leadframe and a first gate attach area along with a second source attach area on a second surface of the leadframe and a second gate attach area. The device also includes two dies, a first of which is coupled to the first source and gate attach areas, while a second of which is coupled to the second source and gate attach areas. A drain connection assembly is coupled to a drain region of the first die and a body is coupled to the semiconductor device such that a drain region of the second die is exposed.

In accordance with one aspect of the present invention, the dies are bumped dies.

In accordance with another aspect of the present invention, the drain connection assembly includes a drain clip and a lead rail adjacent an edge of the drain clip.

The present invention also provides a method of making a semiconductor device.

Other features and advantages of the present invention will be understood upon reading and understanding the detailed description of the preferred exemplary embodiments found herein below, in conjunction with reference to the drawings, in which like numerals represent like elements.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a top perspective view of a semiconductor device in accordance with the present invention;

Figure 2 is a bottom perspective view of a semiconductor device in accordance with the present invention; and

Figure 3 is an exploded view of a semiconductor device in accordance with the present invention.

DETAILED DESCRIPTION OF THE SPECIFIC EXEMPLARY EMBODIMENTS

A semiconductor device 10 includes a leadframe 11, which includes a plurality of leads 12, and a body 13.

In accordance with the present invention, and as can be seen in Figure 3, the leadframe 11 preferably includes a first source attach area 20 on a top surface 21 and a second source attach area 22 on a bottom surface 23 of the leadframe. First and second gate attach areas 24, 25 are included and have at least one lead 12a and 12b extending therefrom, respectively. Preferably, the gate attach areas are separate from the source attach areas. They may, however, be electrically isolated in another manner.

A first die 30 is coupled to first source and gate attach areas 20, 24. Preferably, this is accomplished with solder bumps 31. Likewise, a second die 32 is coupled, preferably with solder bumps 33 to second source and gate attach areas 22, 25.

In accordance with a preferred embodiment of the present invention, dies 30, 32 are bumped dies, which are one-piece items. As can be seen in Figure 4, a bumped die includes the die, an "under bump" material 40 that serves as an intermediate layer between the top surface of the die and solder bump 41, and solder bumps 41 themselves. Preferably, the under bump material is one of TiW, Cu, Au or an equivalent. In the example illustrated in Figure 4, the under bump material is broken into three layers - Cu plating 40a, sputtered Cu 40b, and sputtered Ti 40c.

A drain clip assembly 50 is attached to drain region 51 of the first die preferably with solder. The drain clip assembly includes a top die drain clip 52 and a side rail leadframe 53. Solder paste is dispensed on the drain region of the first die and into elongated v-groove 54 in side rail 53. Clip 50, preferably comprising copper, is supplied, (preferably in reel form) and pick-and-placed onto the die backside such that edge 55 of the copper clip is placed within the elongated v-groove. Thus, the clip provides contact with the first die's drain regions and couples these drain regions to leads 56 of the side rail.

Finally, the package or body 13 is placed around the semiconductor device with the leads exposed therethrough. Preferably, the body comprises a two-piece, molded plastic package.

As can be seen in Figure 2, the bottom of the body includes a window or opening 60 defined therein, thus exposing drain region 61 of the bottom die. Accordingly, when the semiconductor device is used, the drain region of the second die is coupled directly to a circuit board.

As can be seen in Figure 1, leads 62 serve as the common source connections while leads 56 serve as the drain connections for the first or top die. Lead 63 serves as the gate connection for the first die while lead 64 serves as the gate connection for the second die. Parallel connection of the top and bottom dies may be specially routed on the circuit board for optimum electrical performance. Isolating the connections of the top and bottom dies may be an option depending upon the device application.

Preferably, the leadframe comprises copper. As noted above, the top die drain clip preferably also comprises copper.

In accordance with one embodiment of the present invention, a semiconductor device is manufactured by flipping the second or bottom die onto the source and gate attach areas with pre-dispensed flux to facilitate the first pass reflow process. The solder bumps are then reflowed to couple the die to the leadframe. The leadframe with the bottom die will then undergo a second flip chip attach process. This second flipchip attach process takes care of the top die connection to its designated source and gate areas. This will likewise, undergo a second pass reflow which is done at a lower temperature compared to the first pass so that the solder of the first flipchip attach process does not reflow. The drain clip is then flipped onto the drain region of the top die. The drain clip attachment is done at a temperature lower than the second pass reflow process to prevent the previous solder additions from reflowing. The drain clip connection may be accomplished by a solder paste or a conductive adhesive. The body is then placed around the semiconductor device. As noted previously, preferably the

body is a piece molded package. The two pieces are preferably coupled to one another through a transfer molding process.

As is known in the industry, the semiconductor device is then completed by degating, debarring and dejuncting the semi-completed semiconductor device. The semiconductor device is deflashed, the body is marked, if desired, and the leads are plated. The leads are also trimmed and formed.

In accordance with an alternative embodiment of the present invention, the semiconductor device is manufactured in a substantially similar manner. However, instead of reflowing the solder upon placement of the top or first die on the source and gate attach regions, the solder is not reflowed until after the drain clip is placed on the drain region of the top die. Thus, the solder bumps between the top die and the leadframe with pre-dispensed solder paste in between them and the drain clip and the top die, also with pre-dispensed solder paste between them, are reflowed at the same time. Other conductive adhesives can be used as an alternate to the solder paste.

Thus, the present invention provides a semiconductor device that includes two dies stacked with the leadframe therebetween, thus providing a common source region. Such a parallel connection of the first and second chip doubles the silicon performance of the largest chip that generally may be accommodated in typical semiconductor packages while maintaining generally existing package layouts.

Generally, since two chips are accommodated inside the package, the total affected chip size equivalent to approximately 16.8 square millimeters. This generally equates to a 30 percent increase in the number of trench cells within the package, which generally translates to better RoSon and thermal performance.

Although the invention has been described with reference to specific exemplary embodiments, it will be appreciated that it is intended to cover all modifications and equivalents within the scope of the appended claims.